

# High Performance - Software Defined Radios

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# Waveform HAL Goals to achieve Maximum Portability between SCA Compliant JTR Sets

- Waveform Specification must be:
  - Vendor Independent (tools, chips, architecture)
  - Hardware Implementation (Resource) Independent
    - The specification should not imply a specific implementation, or limit changing capabilities.
  - Technology Generation Independent
    - The specification should live through many generations of technology. Today's FPGA implementation may run on a GPP in the future.
  - Executable to allow Validation of Implementation
    - An executable specification allows bit exact implementation validation and A/B performance comparisons of the implementation to the spec to validate function and performance.
  - Consistent with Current Industry Development Methodologies
    - Developers work in signal processing tools: MATLAB/Simulink, RTL (VHDL, Verilog), Rational Rose UML / XML and logic simulation tools. A Specification must be consistent with these tools and methods.

# Waveform HAL Goals to achieve Maximum Portability between SCA Compliant JTR Sets

- HAL API Interface must:
  - Provide practical API (BIOS) interfaces for RF & analog processes
    - Set freq, BW, sample rate, time slot timing, AGC, ALC, antenna management, PA management, etc
  - Provide high performance connectivity between computational resources
  - Interface to SCA services & OS
  - Support High Performance Waveforms
    - Overhead, latency must be consistent with High Performance
  - Meet national and international defense requirements
  - Be supported and adopted by international industry as best practice
  - Must be standardized

# Waveform HAL Goals to achieve Maximum Portability between SCA Compliant JTR Sets

- General Dynamics has recommended a process for updating SCA and HAL development that works with SDR Forum to assure industry buy-in. This recommended process is duplicated here from our SCA proposals.
- General Dynamics Strongly Recommends use of OMG Specifications on how to specify real time performance requirements
  - OMG UML Profile for Schedulability, Performance and Time [1],
  - OMG Real-Time CORBA (Dynamic Scheduling) specification [2].
- High Performance Waveforms can be implemented with FPGA signal processing to meet performance needs of GIG comms elements
  - SDR architectures can be extended to these data rates while retaining waveform extensibility and SCA compliance
  - MATLAB/Simulink is current best choice of waveform specification and interoperability test databases
    - Generates both C and VHDL outputs
    - Broad interoperability with mainstream component vendors
- High Performance Corba is possible and is demonstrated by GD within the DMR, and is available from PrismTech as a COTS product

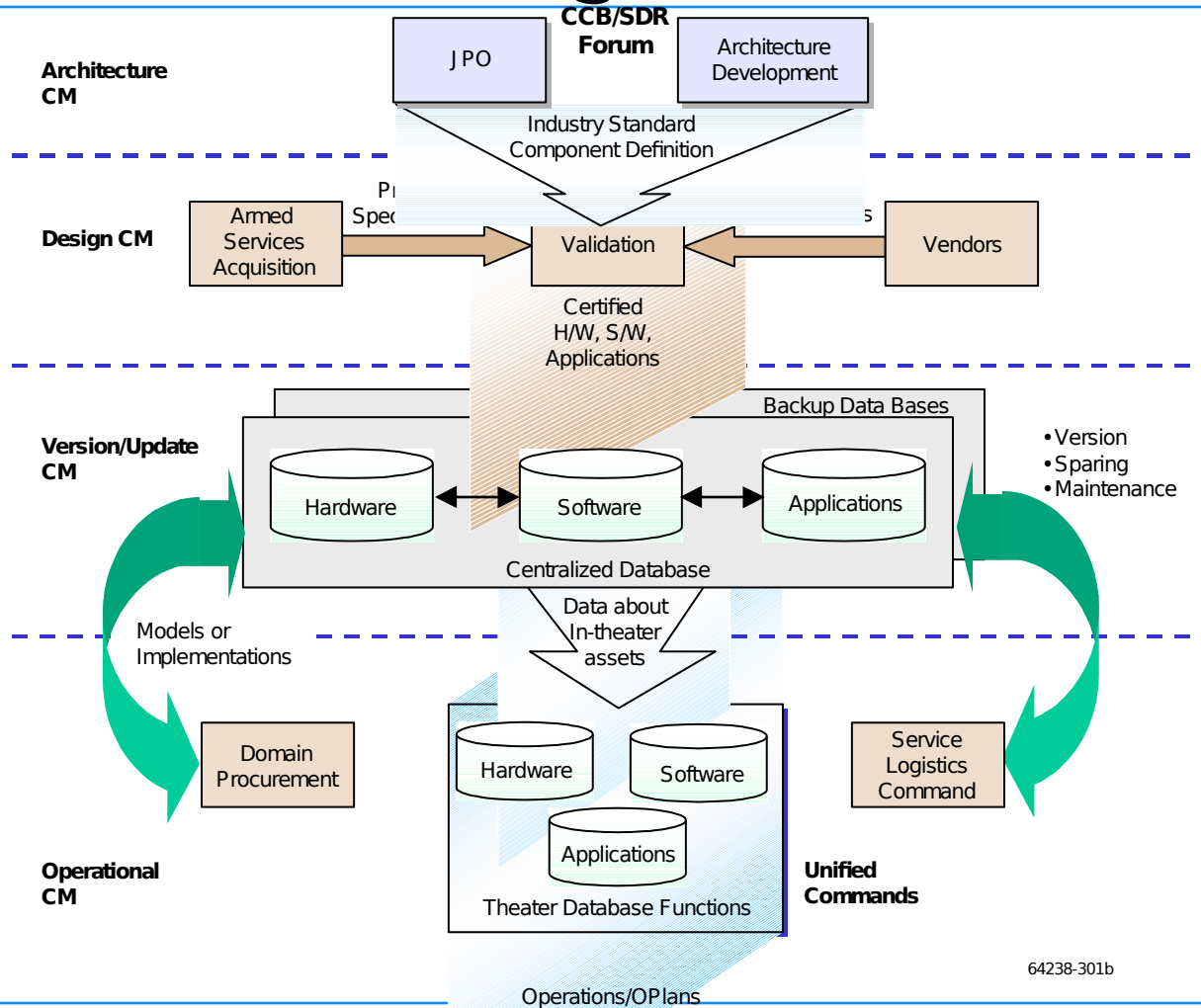
# HAL - The End Game

## (where do we want to be in 5 years)

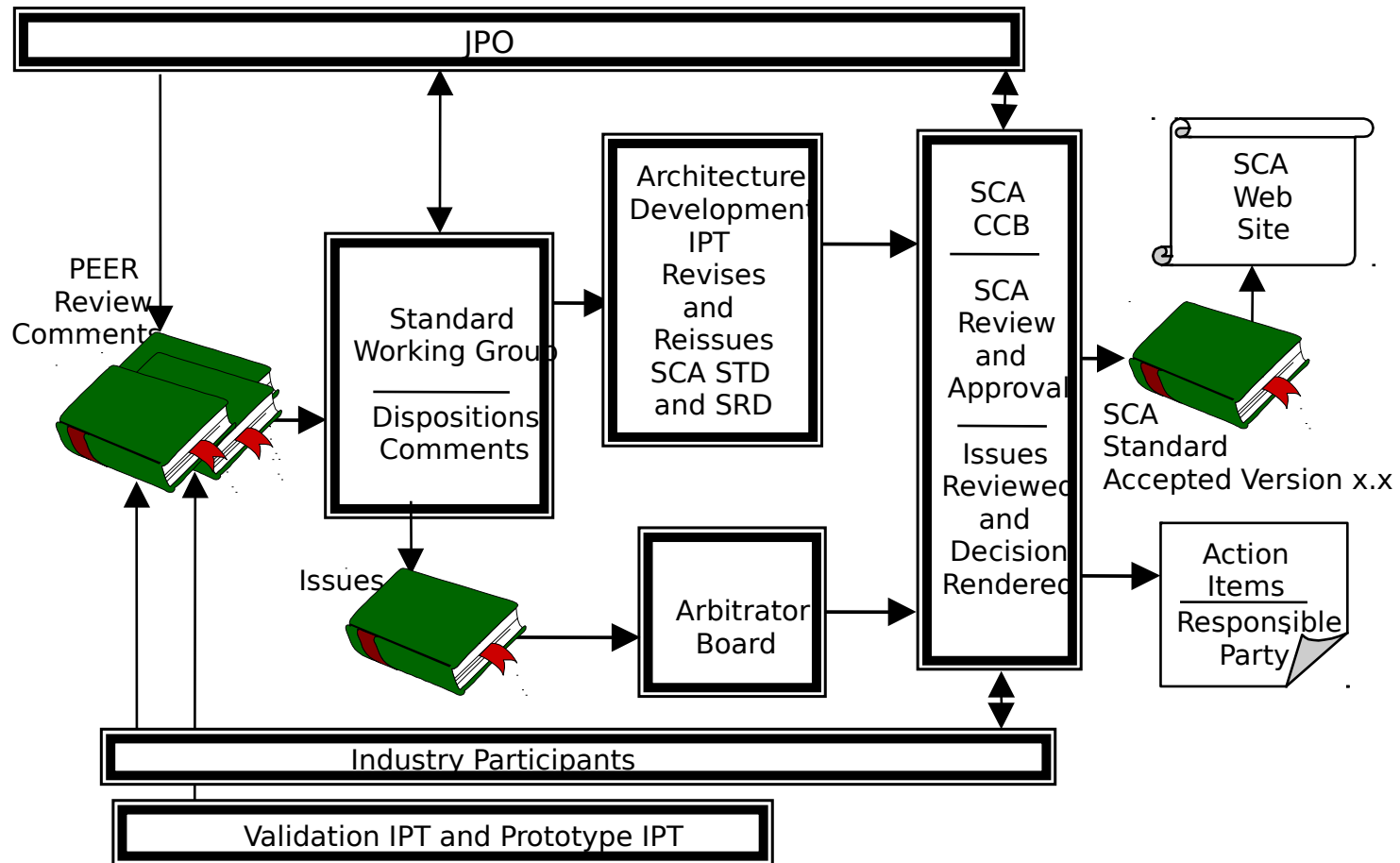
- The Ultimate Goal of the HAL Is to Provide True WF Portability. Presuming a Reasonable Maturation Process for the HAL and Its Constituents, The Following Observations Could Be Made:
  - WFs Will Be Designed and Implemented in Terms of the SCA/HAL Representations of Threads, Devices, Transports, and the Quality of Service Expectations for Each.
  - Platforms Will Be Designed and Implemented to Support the SCA/HAL Representations of Threads, Devices, Transports, and the Available Quality of Service Levels for Each.
  - The Process for Instantiating and Executing a WF on a Given Platform Will Be a Negotiation of Performance Availability
    - A WF may be able to execute on a poorly performing platform with only a subset of its available modes (e.g. no frequency hopping mode), or
    - A WF may “announce” that it cannot execute on a poorly performing platform at all.

# Recommended Industry Participation Process for SCA and HAL API

# JTRS SCA Configuration Management

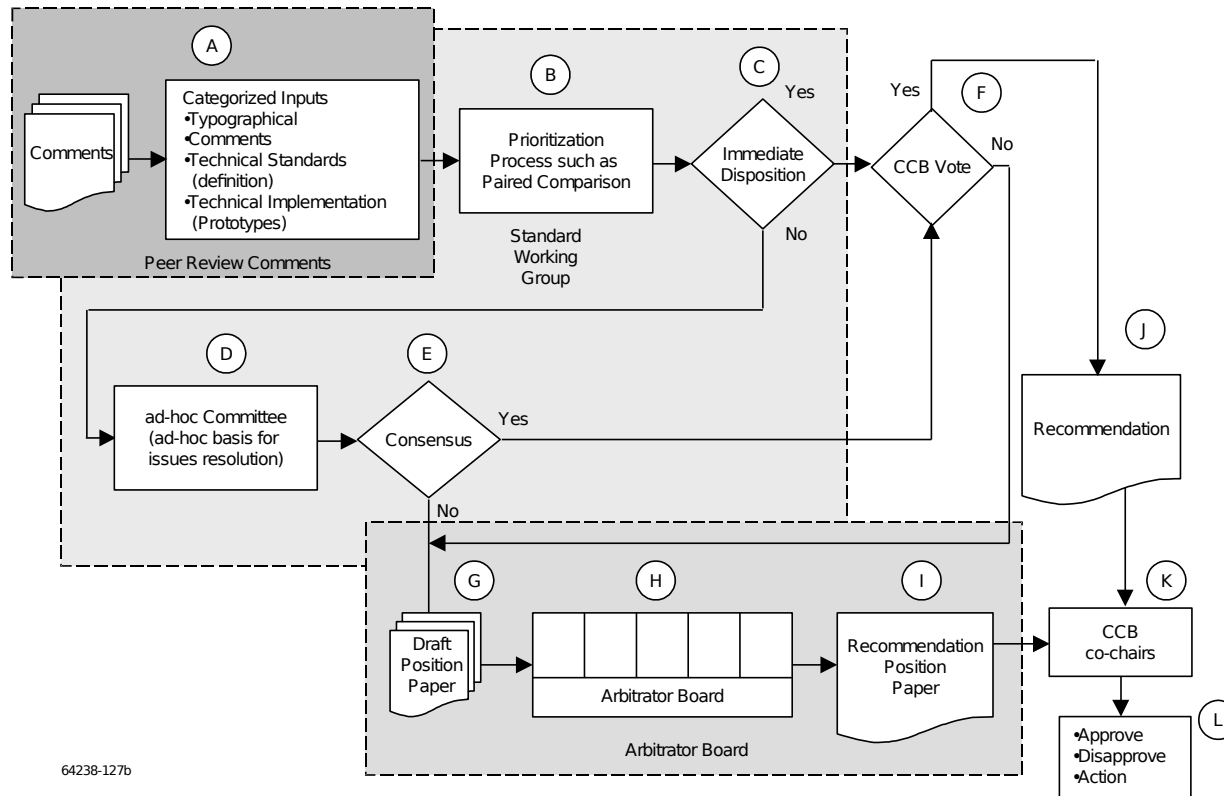


# SCA Maturation

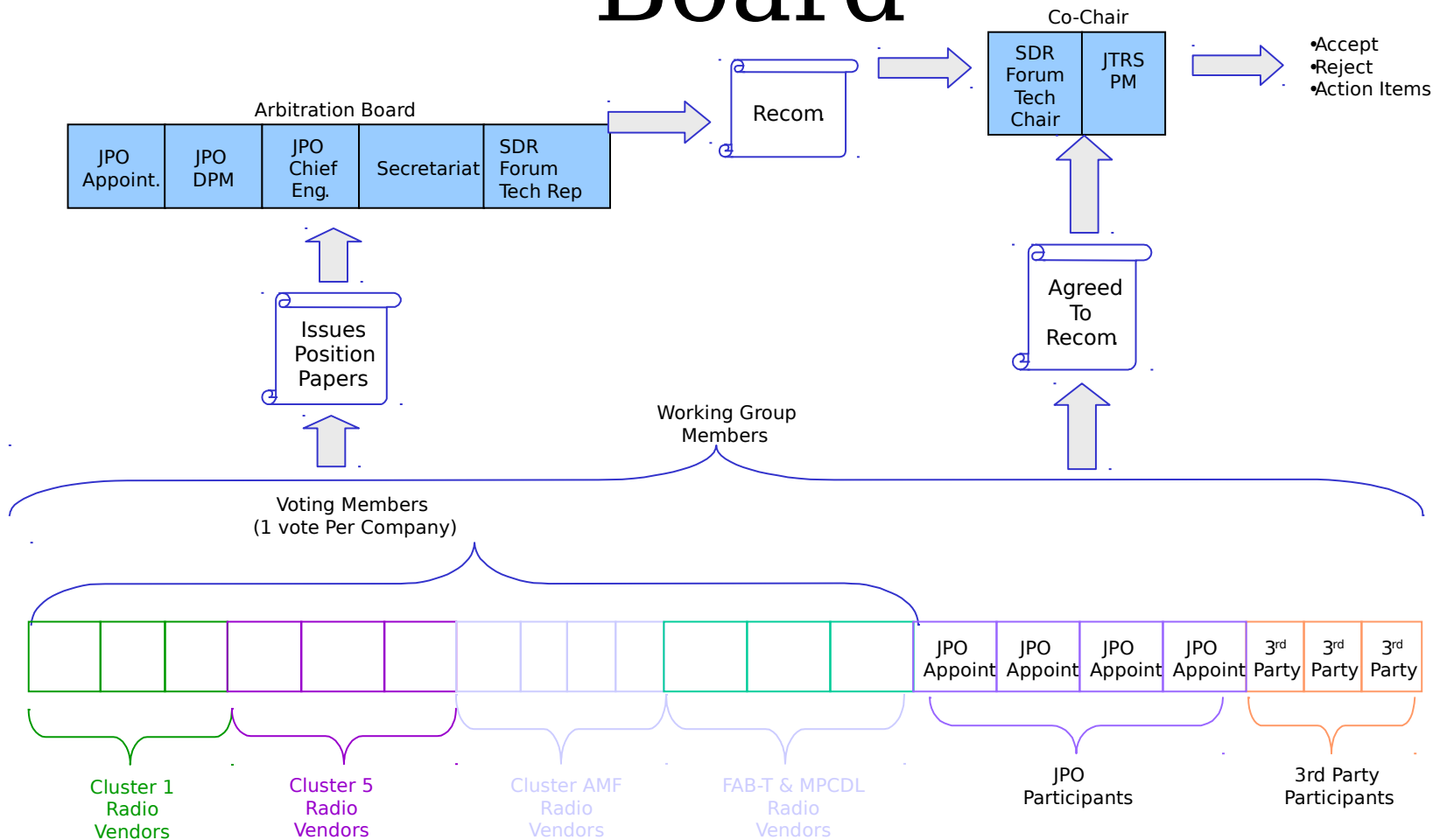




# CCB Process Flow

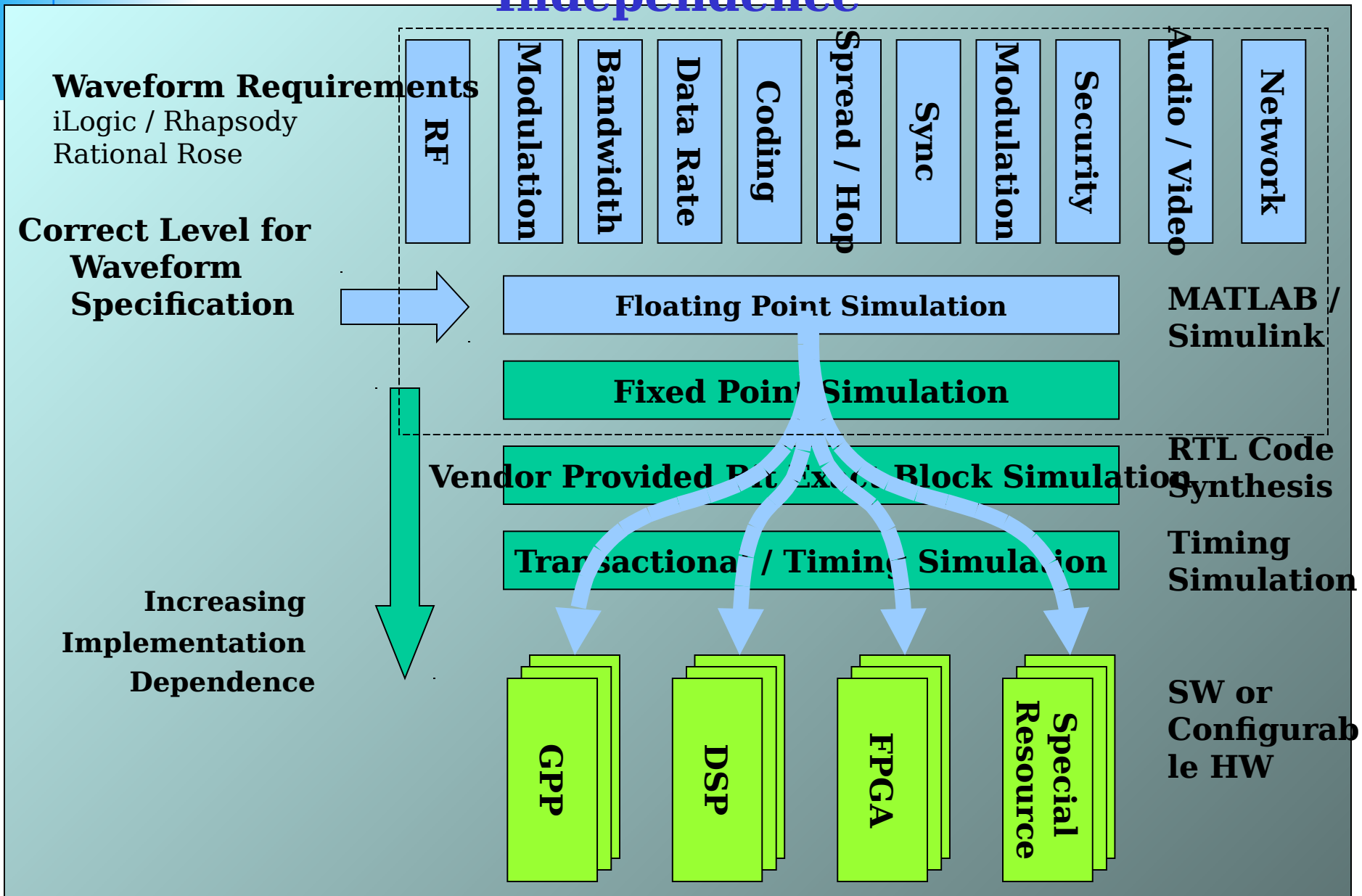


# Configuration Control Board



# Visualization of Waveform Specification Flowdown from MATLAB/Simulink to GPP, DSP, FPGA or Custom LSI Computational Resources

# Maximum Portability Demands Implementation Independence



FPGA Sig Proc Resources Provide  
Sufficient Throughput To Enable  
GIG Performance Levels - While  
Retaining SCA Compliant  
Architecture

# FPGA - High Speed Performance

- 5 Tap Equalizer - 200 Mhz BW
- Reed Solomon (255,223) 8 bit symbols ; clock rate = 124 Mhz ; throughput= 992 Mbps  
[www.xilinx.com/ipcenter/catalog/logicore/docs/rs\\_decoder.pdf](http://www.xilinx.com/ipcenter/catalog/logicore/docs/rs_decoder.pdf)
- Vitterbi Decoder (K=9) Soft decision; clock rate = 141 Mhz; throughput =141 Mbps  
[www.xilinx.com/ipcenter/catalog/logicore/docs/viterbi.pdf](http://www.xilinx.com/ipcenter/catalog/logicore/docs/viterbi.pdf)
- SERDES I/O > 1Gbps x 4

# General Dynamics Contribution of HAL to SDR Forum HAL WG

# General Dynamics HAL WG Contribution - Objective

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- Objective is an Open Standard API so that all waveforms developed by industry are portable to arbitrary HW & SW framework
- What it is and is not:
  - Must not include any industry proprietary components
  - Must be published and available for use in Industry Best Practice Waveform Reference



# General Dynamics' HAL WG Contribution

- The function of the HAL is to remove the dependency of an SCA compliant waveform upon the underlying radio hardware. It should be feasible, through maturation of the HAL and its underlying implementations, to provide a waveform execution environment transparent to the radio hardware.

# General Dynamics - HAL Architecture Requirements

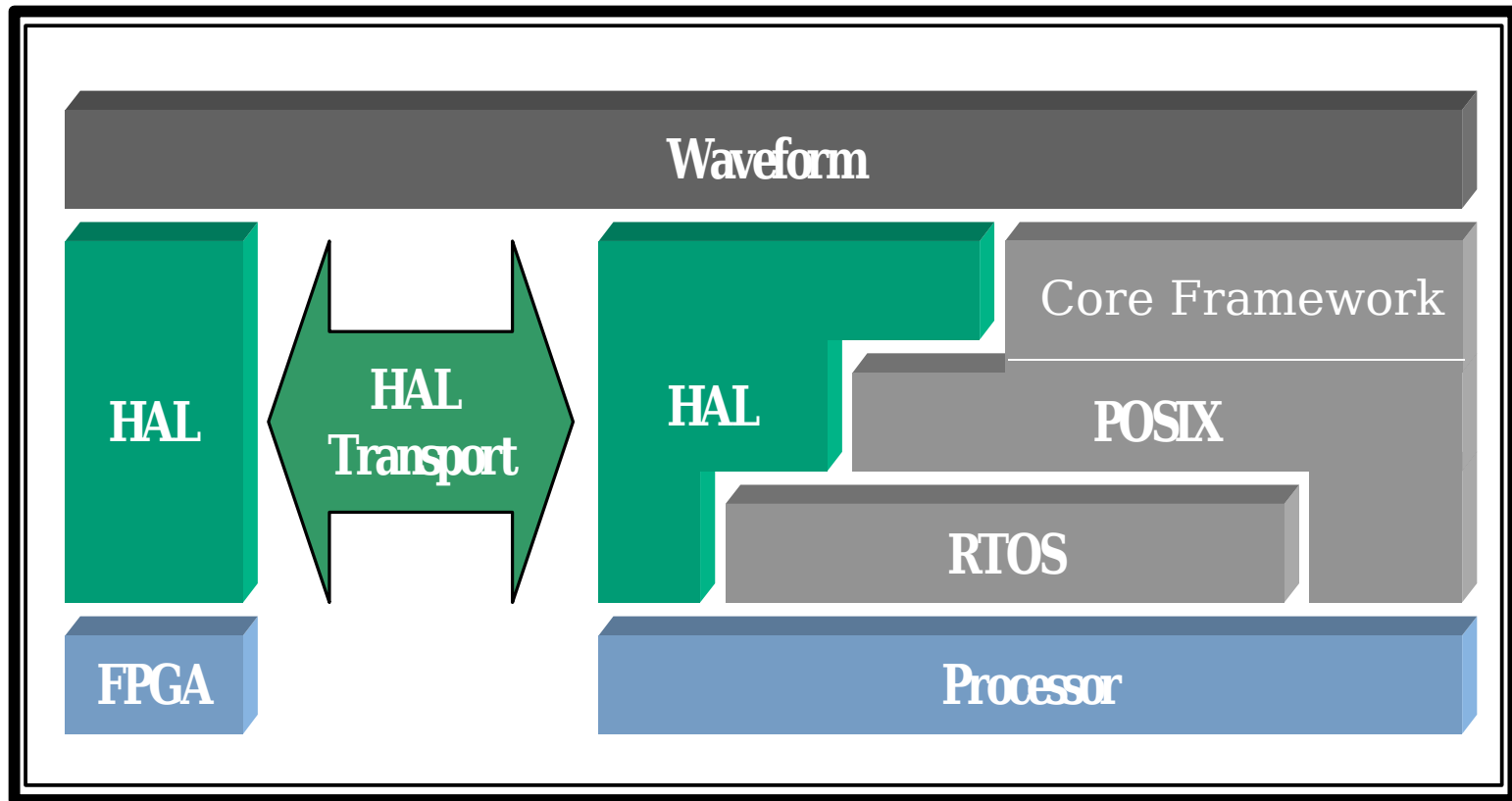
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- HAL must require interface and processing homogeneity across various heterogeneous computing platforms which may be contained within an SDR.
- Present in entire Representative SDR Set in a consistent manner thereby encompassing both the SPS and the HPLS.
- The Device type (after the application of the HAL) will need to correspond 1:1 to all throughput/bandwidth impacting devices present on the platform (e.g., GPP, DSP, FPGA, Busses, etc).

# Important HAL Requirements

- The consideration of platform transport services as an integral part of the HAL can not be over emphasized.
- Ensure that the transport services support the required transport delay and jitter when interfacing with a link layer process running on a GPP. A long delay time or significant variation in bit (packet) transfer can cause the waveform to not function and / or to require the addition of bit (packet) buffering to function properly at an increase in the overall latency.

# Block Diagram HAL relative to HW & SW Framework

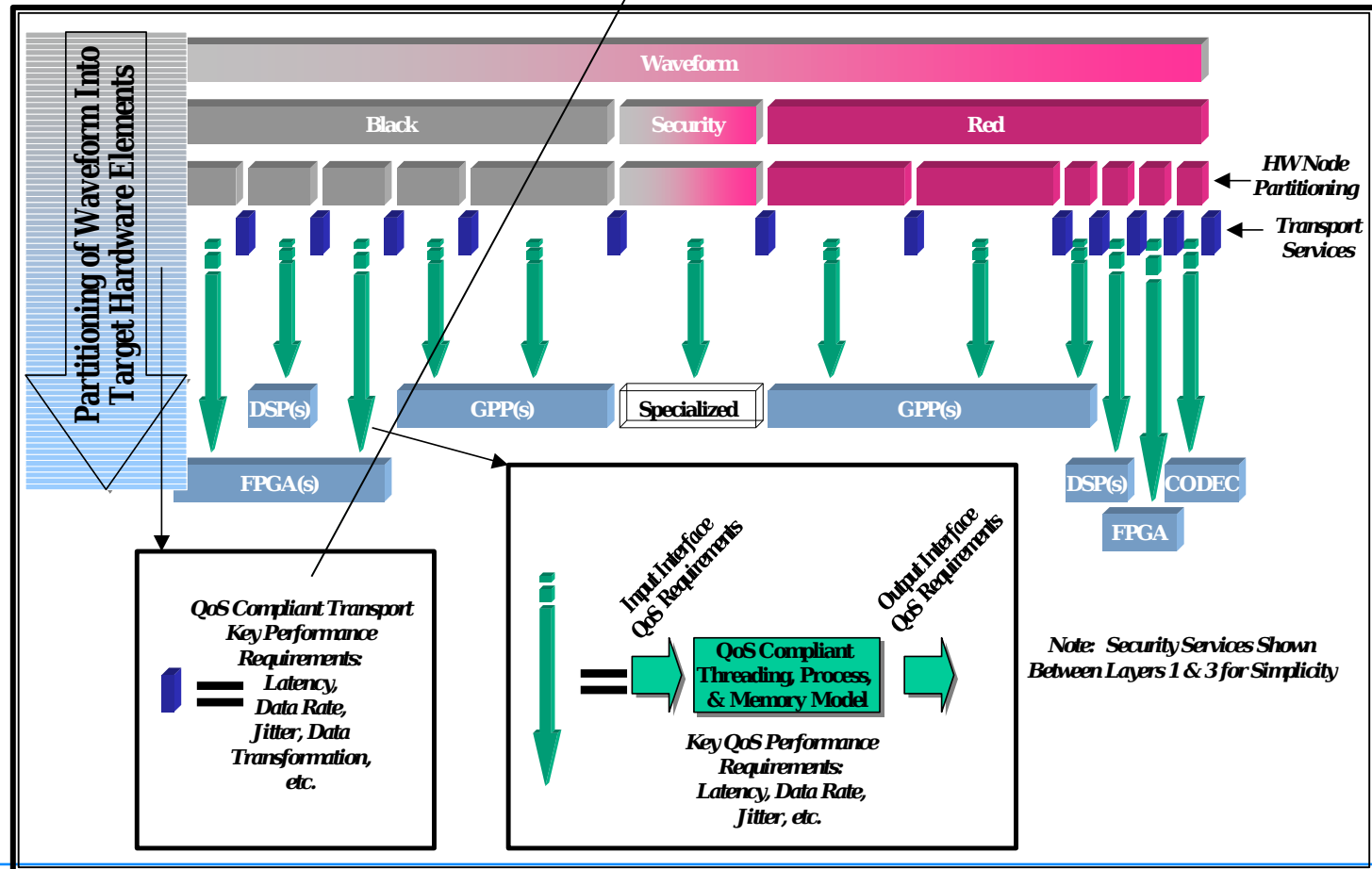


# HAL API

- **HAL is only an API - A specification of a Common Interface**
- Modeled in UML, the HAL takes the form of additional classes (TimeValue, ClockInterrupt, ActionExecution, QoSvalue, Instance, etc.)
- Inheritance modifications to existing classes (e.g., Resource, Device, etc.) provide a richer set of interfaces and associated semantics across the entire SCA model enabling communication of QoS requirements for waveforms.
- HAL provides a consistent threading, process, and memory model which may or may not comply with the model present in the underlying RTOS

# Waveform Objects

This is critical!



# General Dynamics has demonstrated use of real time CORBA Implementations in SDR

- Our RT ORB has been made commercially available through Prism Tech

# Required Realization Standards Exist in OMG

- Leverage two existing Object Management Group (OMG) specifications:
  - the OMG UML Profile for Schedulability, Performance and Time [1],
  - and the OMG Real-Time CORBA (Dynamic Scheduling) specification [2].
  - Additional work will need to be performed for interfaces which do not leverage CORBA (e.g. FPGAs & Security boundaries) as QoS constraints at the CORBA interfaces will propagate into underlying implementations.
  - A Rational Rose model which leverages these specifications by augmenting the current Joint Tactical Radio System (JTRS) Software Communications Architecture (SCA) specification is currently under development by General Dynamics and will be provided at a later date to the SDR Forum for consideration. This model will demonstrate the application of the OMG standards [1,2] into the SDR domain along with the modeling techniques needed to introduce QoS definitions, a consistent adaptation of threading and process, a standard representation for time & task scheduling, and extend the current minimum CORBA specification to embrace the real time demands placed upon SDRs.



# References

- [1] OMG UML Profile for Schedulability, Performance, and Time, v1.0, 09/01/2003, available online at <http://www.omg.org/cgi-bin/doc?formal/2003-09-01> [Link](#)
- [2] OMG Real-Time CORBA (Dynamic Scheduling) specification, version 2.0, 11/01/2003, available online at [http://www.omg.org/technology/documents/formal/RT\\_dynamic.htm](http://www.omg.org/technology/documents/formal/RT_dynamic.htm) [Link](#)
- [3] Platform Independent Model (PIM), available online at <http://groups.yahoo.com/group/srsupport/files/Submission Document/20040315>
- [4] IO Facilities (submission) available online at <http://groups.yahoo.com/group/srsupport/files/Submission Document/20040315>
- [5] IO Facilities (as updated by Thales), attached.